

CLAIMS

What is claimed is:

1 1. A COFDM demodulator, comprising:
2 a fast Fourier transform circuit for analyzing a received signal in a window
3 corresponding to one symbol, each symbol carrying several phase and amplitude modulated
4 carriers, some of which, shifted in frequency in a predetermined way from one symbol to the
5 next one, form pilots;

6 a bidimensional filter for interpolating, from anchors corresponding to the pilots
7 such as received from several consecutive symbols, the distortion undergone by each carrier;
8 means for correcting window shifting with respect to an optimal position; and
9 means for correcting each distortion according to window shifting corrections
10 performed respectively for the symbol associated with the distortion and for the symbols
11 associated with the anchors used to interpolate the distortion.

12 2. The demodulator of claim 1 wherein the means for correcting the window
1 shifting comprise a phase-locked loop synchronized on a correlation signal obtained by a
2 correlation product between the received signal and this same signal delayed by one symbol,
3 each symbol being preceded by a guard interval corresponding to a copy of the end of the
4 symbol.
5

6 3. The demodulator of claim 1 wherein each distortion is, in the frequency
7 field after Fourier transform, a weighted sum of two anchors of the same position in a preceding
8 symbol and in a following symbol, to which anchors have been added respective phases
9 corresponding to the shiftings undergone by the analysis window for the preceding and following
10 symbols, and to which anchors has been subtracted a phase corresponding to the shifting
11 undergone by the analysis window for the symbol associated with the distortion.
12

1 ~~7~~ 4. A COFDM demodulator with fast Fourier transform (FFT) analysis
2 window displacement compensation, comprising:

3 a reconstruction circuit configured to receive radio-transmitted signals in a
4 window corresponding to one symbol, the symbol carrying a plurality phase and amplitude
5 modulated carriers, one or more of the carriers are shifted in frequency in a predetermined way
6 from one symbol to the next symbol and form pilots, the reconstruction circuit configured to
7 extract the symbols and convert the symbols into digital signals;

8 an adjustment circuit and an associated phase-locked loop (PLL) circuit
9 configured to receive the digital signals and determine and readjust the position of the
10 corresponding windows;

11 an FFT circuit configured to perform a fast Fourier transform with the windows
12 and output a transformed signal including complex coefficients;

13 a conversion circuit configured to receive a position signal from the PLL and to
14 output a conversion signal that is corrected for distortion;

15 a distortion interpolation circuit configured to receive the transformed signal and
16 the conversion signal and to provide an interpolated distortion signal; and

17 a correction circuit configured to receive the interpolated distortion signal and to
18 output a corrected complex coefficients signal.

1 ~~8~~ 5. The demodulator of claim ~~4~~ ⁷, further comprising a delay circuit coupled
2 between the FFT circuit and the correction circuit and coupled in parallel with the distortion
3 interpolation circuit.

1 ~~9~~ 6. The demodulator of claim ~~4~~ ⁷ wherein the PLL is configured to be
2 synchronized on a correlation signal obtained by a correlation product between the received
3 radio-transmitted signals in a window and this same signal delayed by one symbol, each symbol
4 being preceded by a guard interval corresponding to a copy of the end of the symbol.

1 ~~10~~ 7. The demodulator of claim ~~4~~ ¹⁷ wherein the PLL comprises an accumulator
2 that outputs the absolute position of the window with respect to a corresponding symbol.

1 ~~11~~ 8. The demodulator of claim ~~7~~ ¹⁰ wherein the conversion circuit is configured to
2 convert the absolute position received from the PLL into a form that is usable by the distortion
3 interpolation circuit.

1 ~~12~~ 9. The demodulator of claim ~~4~~ ⁷ wherein the PLL is configured to control the
2 adjustment circuit.

1 ~~13~~ 10. The demodulator of claim ~~4~~ ⁷ wherein the interpolation circuit comprises:
2 first, second, and third anchor input registers coupled to a first multiplexer;
3 fourth, fifth, and sixth anchor input registers coupled to a second multiplexer; and
4 first and second multipliers each having inputs coupled respectively to the first
5 and second multiplexers, and each further having an output coupled to a common adder.

1 ~~14~~ 11. The demodulator of claim ~~10~~ ¹³ wherein the conversion circuit comprises:
2 first, second, and third analysis window shift value registers coupled to a first
3 multiplexer;
4 fourth, fifth, and sixth analysis window shift value registers coupled to a second
5 multiplexer;
6 the first and second multiplexers each having an output coupled to respective
7 inputs of first and second adders;
8 the first and second adders each having an output coupled to respective first and
9 second multipliers;
10 the first and second multipliers each having an output coupled to respective first
11 ~~and second polar-to-cartesian converters; and~~

12 the first and second polar-to-cartesian converters each having an output coupled
13 to respective second inputs of the first and second multipliers of the interpolation circuit.

1 ~~15~~ 12. The demodulator of claim ~~11~~ ¹⁴ wherein the first and second multipliers of
2 the interpolation circuit comprise complex multipliers.

1 ~~16~~ 13. The demodulator of claim ~~11~~ ¹⁴ wherein the interpolation circuit is
2 configured to calculate distortion according to the following:

$$d_{n,k} = \left(1 - \frac{s}{4}\right) A_{n-s,k} e^{j2\pi f_k (w_{n-s} - w_n)} + \frac{s}{4} A_{n+4-s,k} e^{j2\pi f_k (w_{n+4-s} - w_n)}$$

3 where

A is the received anchors,

S is equal to (n modulo 4 - k/3 modulo 4) modulo 4,

n is the symbol number,

k is the window position,

f_k is the frequency corresponding to position k, and

10 w is the absolute window position expressed in time units of the associated
11 window.

1 ~~17~~ 14. A method of fast Fourier transform (FFT) analysis window displacement
2 compensation in a COFDM modulator, comprising:

3 - receiving a radio-transmitted signal in a window corresponding to one symbol, the
4 symbol carrying a plurality of phase and amplitude modulated carriers, one or more of the
5 carriers are shifted in frequency from one symbol to the next symbol to form pilots, and
6 extracting these symbols and converting these symbols into digital signals;

7 receiving the digital signals and determining and readjusting the position of the
8 windows;

9 receiving the windows and performing a fast Fourier transform with the windows
10 and outputting a transformed signal that includes complex coefficients;
11 receiving a position signal and outputting a conversion signal that is corrected for
12 distortion;
13 receiving the transformed signal and the conversion signal and providing an
14 interpolated signal; and
15 receiving the interpolated signal and outputting a corrected coefficient signal.

1 ~~18~~ 18. The method of claim ~~14~~ 11, further comprising receiving the transformed
2 signal and outputting a delayed transformed signal.

3 ~~19~~ 19. The method of claim ~~14~~ 11, further comprising generating a phase-locked
4 loop signal synchronized on a correlation signal obtained by a correlation product between the
5 received signal and this same signal delayed by one symbol, each symbol being preceded by a
6 guard interval corresponding to a copy of the end of the symbol.

7 ~~20~~ 20. The method of claim ~~14~~ 11, comprising calculating distortion according to the
8 following:
9

$$d_{n,k} = \left(1 - \frac{s}{4}\right) A_{n-s,k} e^{j2\pi f_k (w_{n-s} - w_n)} + \frac{s}{4} A_{n+4-s,k} e^{j2\pi f_k (w_{n+4-s} - w_n)}$$

4 where

5 A is the received anchors,
6 S is equal to (n modulo 4 - k/3 modulo 4) modulo 4,
7 n is the symbol number,
8 k is the window position,
9 f_k is the frequency corresponding to position k, and